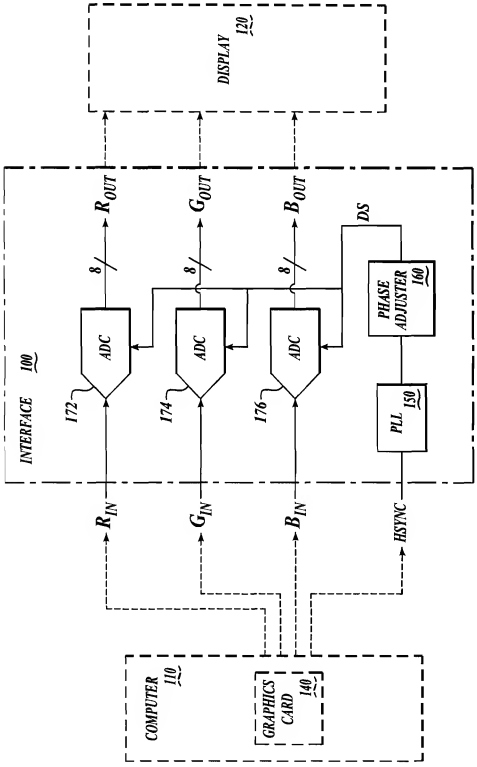

DISPLAY
120
INTERFACE
100
ADC
ADC
ADC
172
174
176
8
8
8
R_{OUT}
G_{OUT}
B_{OUT}
DS
PHASE ADJUSTER
160
PLL
150
R_{IN}
G_{IN}
B_{IN}
HSYNC
COMPUTER
110
GRAPHICS CARD
140

Fig. 1

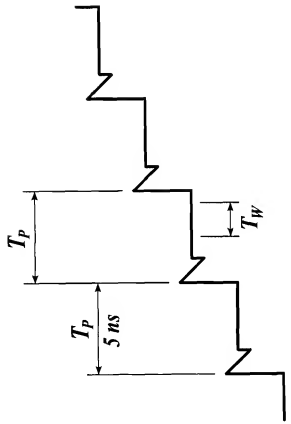


Fig.2

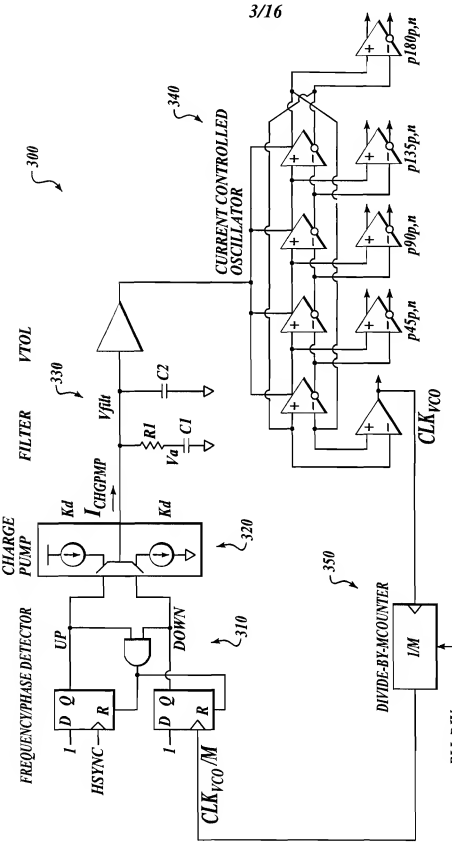

300
FREQUENCY/PHASE DETECTOR
CHARGE PUMP
FILTER
VTOL
CURRENT CONTROLLED OSCILLATOR
340
330
320
310
350
UP
DOWN
Kd
I_{CHGPMP}
Vfilt
R1
C1
C2
Va
CLK_{VCO}
CLK_{VCO}/M
HSYNC
PLL DIV
DIVIDE-BY-MCOUNTER
1/M
/12
p180p,n
p135p,n
p90p,n
p45p,n

Fig.3

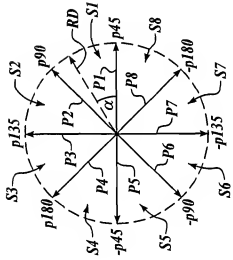

RD
S1
p45
S8
S2
p90
P1
P8
-p180
S7
α
p135
P2
P7
P3
P6
-p135
S3
P4
P5
S6
p180
S4
-p45
S5
-p90

Fig.4

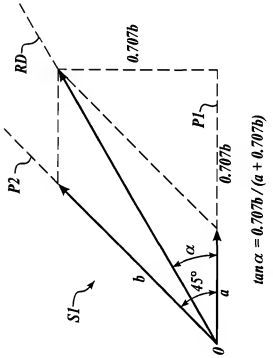


Fig.5

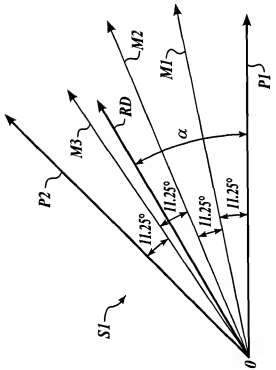


Fig.6

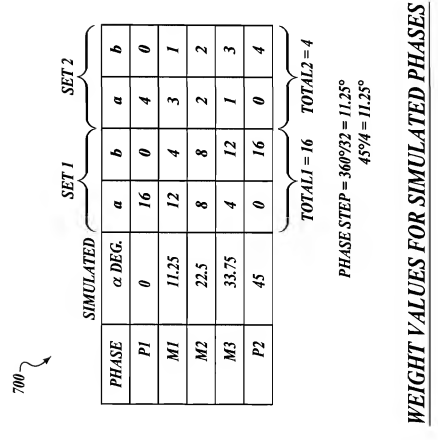
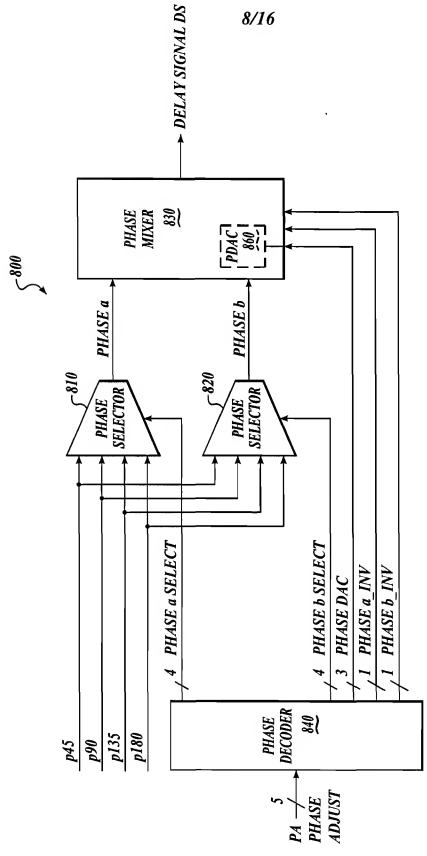

700
SIMULATED
SET 1
SET 2
PHASE
α DEG.
a
b
a
b
P1
0
16
0
4
0
M1
11.25
12
4
3
1
M2
22.5
8
8
2
2
M3
33.75
4
12
1
3
P2
45
0
16
0
4
TOTAL1 = 16
TOTAL2 = 4
PHASE STEP = 360°/32 = 11.25°
45°/4 = 11.25°
WEIGHT VALUES FOR SIMULATED PHASES

Fig. 7



PHASE ADJUSTER

Fig. 8

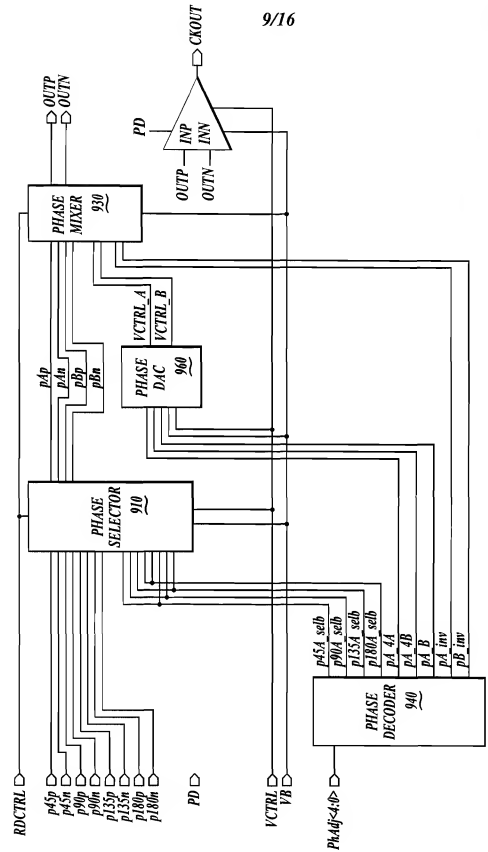
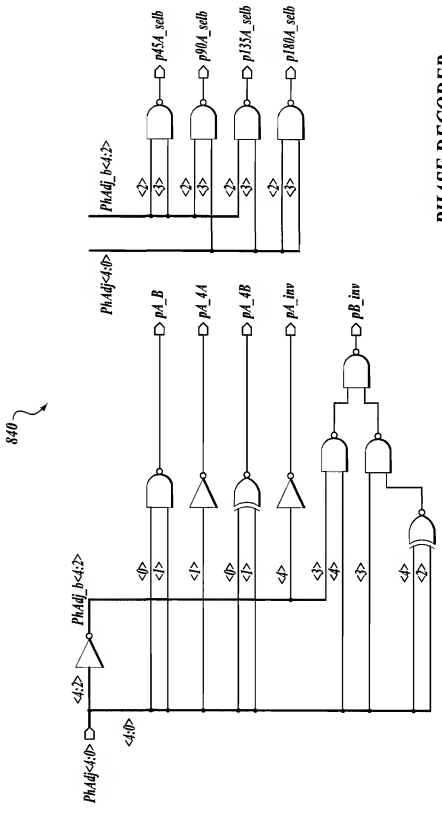

PHASE ADJUSTER IC
RDCTRL
p45p
p45n
p90p
p90n
p135p
p135n
p180p
p180n
PD
VCTRL
VB
Pkadj<4:0>
VDDA
VSSA
PHASE SELECTOR 910
PHASE DECODER 940
PHASE DAC 960
PHASE MIXER 930
PD
INP
INN
OUTP
OUTN
CKOUT
VCTRL_A
VCTRL_B
pAp
pAn
pBp
pBn
p45A_selb
p90A_selb
p135A_selb
p180A_selb
pA_4A
pA_4B
pA_B
pA_inv
pB_inv

Fig. 9



PHASE DECODER

Fig.10

11/16

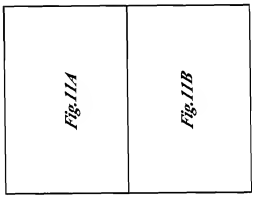
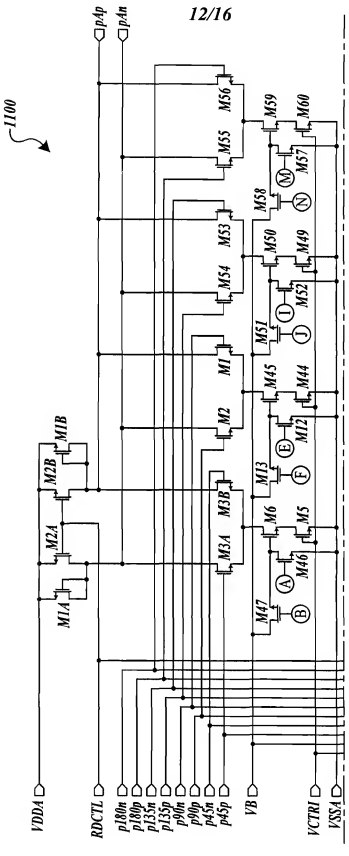


Fig.11



PHASE SELECTOR CHIP

Fig. 11A

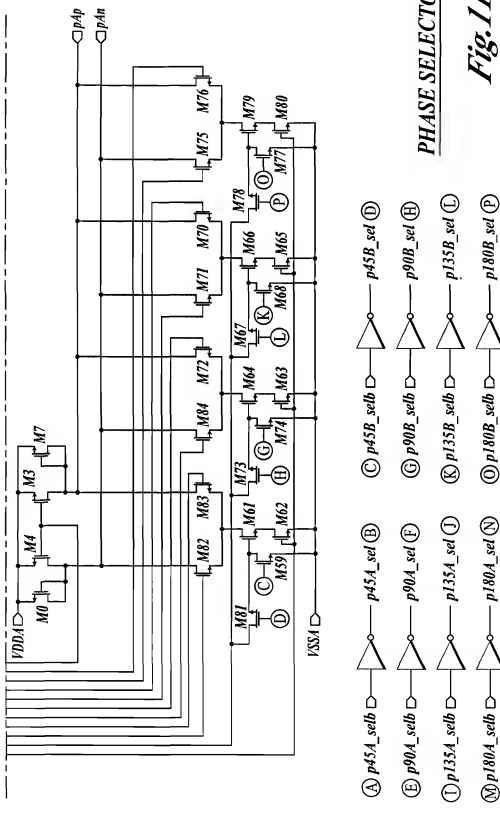
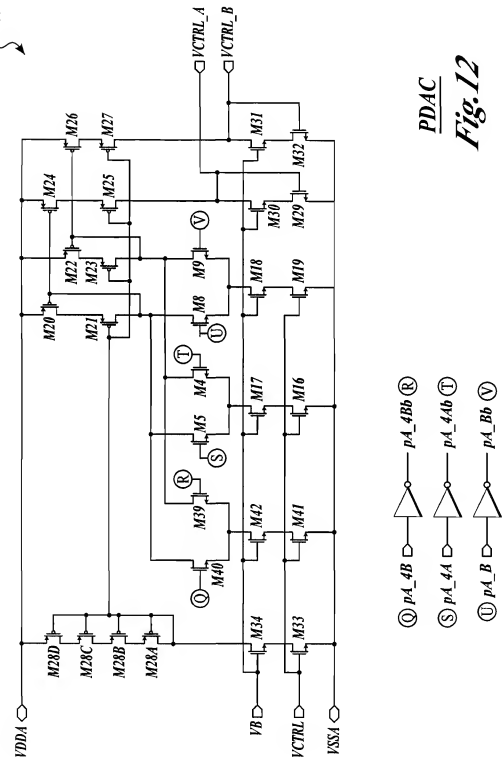

PHASE SELECTOR CHIP
VDDA
VSSA
pAp
pAn
M0
M4
M3
M7
M82
M83
M61
M73
M84
M72
M64
M63
M74
M62
M59
M81
M75
M76
M79
M80
M77
M78
M70
M71
M66
M65
M67
M68
A p45A_selb
E p90A_selb
I p135A_selb
M p180A_selb
B p45A_sel
F p90A_sel
J p135A_sel
N p180A_sel
C p45B_selb
G p90B_selb
K p135B_selb
O p180B_selb
D p45B_sel
H p90B_sel
L p135B_sel
P p180B_sel

Fig. 11B


1200
VCTRL_A
VCTRL_B
M26
M27
M31
M32
M24
M25
M30
M29
M22
M23
M9
M18
M19
M20
M21
M8
M4
M17
M16
M5
M39
M42
M41
M40
M34
M33
M28D
M28C
M28B
M28A
VDDA
VB
VCTRL
VSSA
pA_4B
pA_4Bb
pA_4A
pA_4Ab
pA_B
pA_Bb

PDAC

Fig. 12

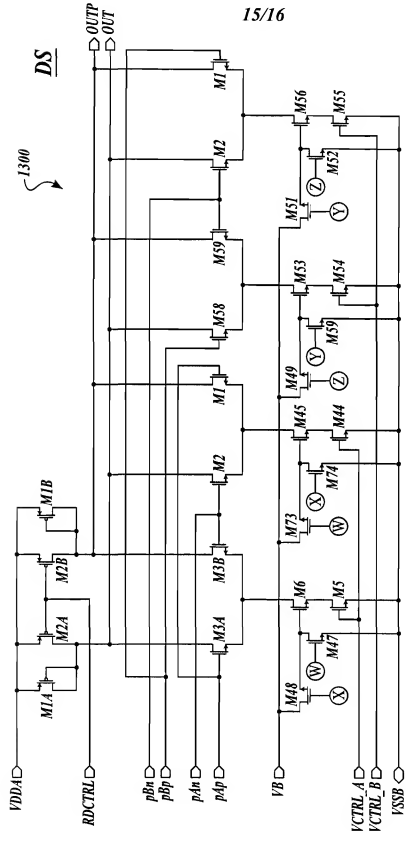

DS
1300
OUTP
OUT
VDDA
RDCTRL
pBn
pBp
pAn
pAp
VB
VCTRL_A
VCTRL_B
VSSB
M1A
M2A
M1B
M2B
M3A
M3B
M1
M2
M58
M59
M6
M5
M47
M48
M73
M74
M45
M44
M49
M1
M2
M58
M59
M53
M54
M39
M51
M52
M56
M55
pA_invb
pB_invb
pA_inv
pB_inv

Fig. 13

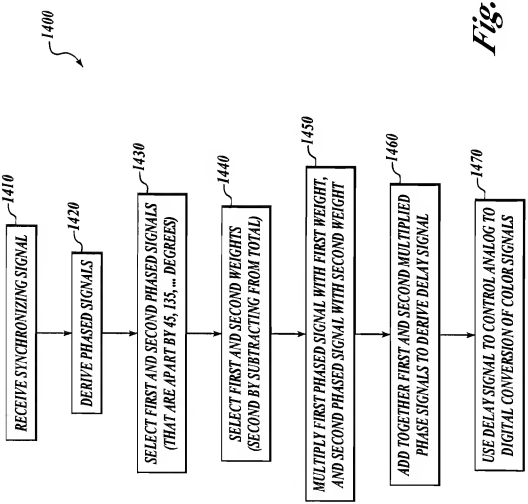

1400
1410
RECEIVE SYNCHRONIZING SIGNAL
1420
DERIVE PHASED SIGNALS
1430
SELECT FIRST AND SECOND PHASED SIGNALS (THAT ARE APART BY 45, 135, ... DEGREES)
1440
SELECT FIRST AND SECOND WEIGHTS (SECOND BY SUBTRACTING FROM TOTAL)
1450
MULTIPLY FIRST PHASED SIGNAL WITH FIRST WEIGHT, AND SECOND PHASED SIGNAL WITH SECOND WEIGHT
1460
ADD TOGETHER FIRST AND SECOND MULTIPLIED PHASE SIGNALS TO DERIVE DELAY SIGNAL
1470
USE DELAY SIGNAL TO CONTROL ANALOG TO DIGITAL CONVERSION OF COLOR SIGNALS

Fig.14